Chip-Level Waveguide-Mirror-Pillar Optical Interconnect Structure

O. O. Ogunsola, *Student Member, IEEE*, H. D. Thacker, *Member, IEEE*, B. L. Bachim, M. S. Bakir, *Member, IEEE*, J. Pikarsky, T. K. Gaylord, *Fellow, IEEE*, and J. D. Meindl, *Life Fellow, IEEE*

***Abstract*—Waveguides, mirrors, and polymer pillars can be integrated together to provide optical interconnects to the chip level. Total internal reflection in the polymer pillar provides a high level of spatial confinement of the light. The metallized mirror terminating the waveguide may be at 45° or at a nearby angle such as 54.74° (anisotropically etched silicon) and produce nearly equal coupling efficiencies. For a polymer waveguide, a gold mirror, and a polymer pillar of the dimensions fabricated, the simulated coupling efficiencies are 80.7% or 0.93 dB (45° mirror) and 82.5% or 0.84 dB (54.74° mirror), respectively. These simulations together with the fabrication and testing of a 54.74° mirror configuration demonstrates the viability of the waveguide-mirror-pillar structure, its insensitivity to mirror angle, and its compatibility with current substrate fabrication technologies.**

***Index Terms*—Finite-difference time-domain (FDTD), mirrors, optical interconnects, optical waveguides, polymer pillars.**

I. Introduction

As microprocessor technology improves towards gigascale integration (GSI), optical interconnects are speculated to help provide high input–output (I/O) bandwidth between a package-substrate and a chip [1]–[5]. For this to occur, schemes for out-of-plane coupling between a substrate and a chip that are compatible with conventional electrical I/O interconnects must be examined. One example scheme bonds active device arrays and a microprocessor onto an interposer that is, in turn, bonded onto a board with mirror-terminated waveguides [2]. A second scheme bonds dissimilar-material chips on a substrate with volume-grating couplers and compliant interconnects [3]. These are quasi-freespace solutions since the light propagating between the substrate and chip is not spatially confined. This necessitates using large lenses (230-μm diameter [2]) and couplers (500-μm length [3]) to account for 1) alignment tolerances due to assembly and 2) the coefficient of thermal expansion mismatch between the package-substrate and chip. In an attempt to address these compatibility and packaging constraints, polymer pillar chip I/O interconnects were introduced [6], [7].

A polymer pillar is a compliant cylindrical structure batch-fabricated at the wafer level after back-end-of-line processing. Each die is flip-chip bonded onto a package-substrate to provide optical I/O interconnection with area densities that can exceed $10^5/\text{cm}^2$ [6]. Air-clad pillars are known to confine and concentrate light [7]; thus, they provide spatial confinement of light in the region between the substrate and chip. To enable them as optical I/O, light is coupled into the pillar using mirror-terminated waveguides, as shown in Fig. 1. The waveguides are embedded in air to provide high index contrast. The figure shows two possible configurations. In Fig. 1(a), the mirror is fabricated by imprinting [8] an anisotropically etched silicon mold with smooth 54.74° slanted sidewalls into the cladding material. In Fig. 1(b), the substrate is a silicon carrier [9] and the mirror is etched directly into it [10]. In both configurations, the mirror angle is not 45° yet it combines with the waveguide and pillar to produce a 90° redirection of the light. Advantages of spatial confinement due to the pillar include 1) smaller optoelectronic device cross sectional dimensions, 2) mirror-angle insensitivity, and 3) compatibility with available substrate fabrication technologies. The motivation for our work is to integrate substrate-level waveguides and mirrors with polymer pillars to enable an optical interconnect structure to serve as a chip-substrate optical I/O. We demonstrate waveguide-to-mirror-to-pillar coupling through simulation and experiment.

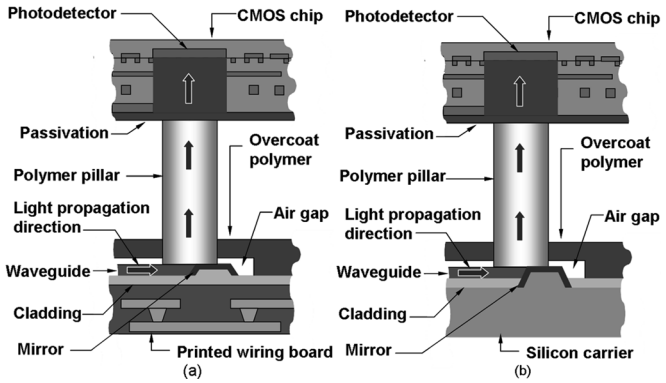

Fig. 1. Schematic of out-of-plane coupling in which mirror-terminated waveguides are integrated with polymer pillar I/O interconnects for coupling light into complementary metal–oxide–semiconductor (CMOS) chips with monolithically integrated CMOS-compatible photodetectors where (a) represents a mirror fabricated by imprint lithography on a printed wiring board and (b) represents a mirror etched directly into a silicon carrier. The package-substrate could alternatively be any multichip module or carrier. The passivation could be any CMOS compatible dielectric material.

II. Optical Spatial Confinement

Optoelectronic devices are generally located directly above their corresponding coupling elements. In geometrical optics, mirrors reflect rays with angles of reflection equal to the angle of incidence. Thus, a 45° angle is the intuitive choice for a mirror to

Manuscript received December 5, 2006; revised May 9, 2006. This work has been carried out as part of the Microelectronics Advanced Research Corporation (MARCO)/Defense Advanced Research Projects Agency (DARPA) Interconnect Focus Center Research Program at Georgia Institute of Technology under Contract 2003-IT-674.

The authors are with the Microelectronics Research Center and the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: gt7100c@prism.gatech.edu).

Digital Object Identifier 10.1109/LPT.2006.879533

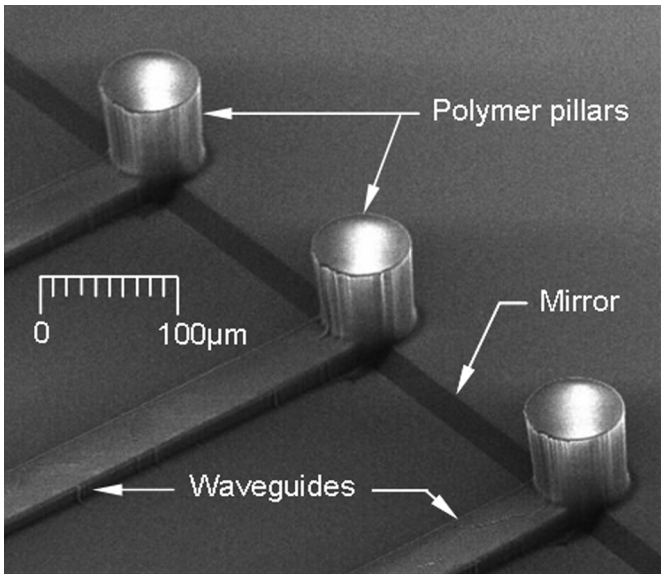

Fig. 2. SEM image of an array of polymer pillars fabricated directly above mirror-terminated waveguide regions.

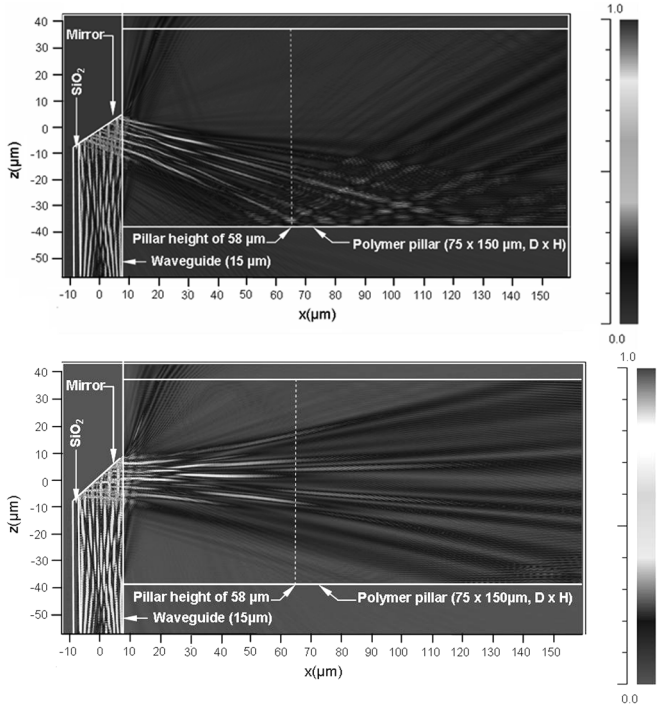

Fig. 3. Time-averaged TE continuous-wave simulation result for waveguide-to-pillar coupling using (a) a metallized silicon mirror that is at a 54.74° angle and (b) a 45° mirror. In both cases, the pillars are in air as shown in Fig. 1. The fabricated pillar's height is shown by a dashed line.

couple light out of a waveguide at 90°. Example 45° mirror-terminated waveguide work for chip-substrate I/O interconnection include [2], [4], and [5]. In [2] and [4], the mirror is formed by dicing, while in [5], the mirror is direct laser-written. However, such fabrication technologies can produce rough surfaces at incorrect angles [4]. These fabrication tolerances can be accounted for by using a polymer pillar. Since an air-clad polymer pillar has a high index contrast ($\Delta n = 0.52$), light coupled into it is confined along its height. Spatial confinement is advantageous as described above. In addition, intentional and unintentional deviations from 45° mirrors can be accounted for while still producing an out-of-plane 90° redirecting of the light. In this work, the coupler is isolated and waveguide-to-mirror-to-pillar coupling using a metallized anisotropically etched silicon sidewall is examined to determine the spatial confinement effect due to the pillar. The fabricated coupler investigated is shown in Fig. 2. Metallized (111) sidewalls on $\langle 100 \rangle$-Si substrates are chosen as the mirror surface because they are smooth and are consistently produced at a 54.74° angle with respect to the substrate surface [11]. Their root-mean-square roughness was measured using an atomic force microscope to be consistently less than 12 nm, which agrees with the values in [11].

III. Simulation

Simulations were performed with FullWAVE finite-difference time-domain (FDTD) software from RSoft Design Group. Simulation parameters were dictated by fabrication capabilities. A two-dimensional FDTD continuous-wave simulation was performed on a 15-μm-tall Avatrel waveguide that terminates at a gold-coated Si mirror beneath a 150-μm-tall air-clad Avatrel pillar. At the simulation and optical test wavelength, $\lambda = 632.8$ nm, Avatrel has a refractive index of 1.52, and Au has a refractive index of $0.2 + j3.32$. The imaginary part of the refractive index corresponds to the finite conductivity and thus losses that gold exhibits at this wavelength. While only a 58-μm-tall pillar was fabricated, the taller pillar was simulated to better illustrate the effect of spatial confinement. Transverse-electric (TE) polarization was chosen since it is commonly used experimentally. The boundaries were perfectly matched layers. The waveguide cladding layer was 2 μm of SiO_2. The substrate-level waveguide's 20 modes were launched with equally distributed power. This was done because experimentally, a single-mode fiber was used to couple light into a 0.5-cm-long waveguide, and simulations show this to be a sufficient length to excite all of these modes. The coupled power was monitored inside and outside of the pillar.

The simulation result for waveguide-to-mirror-to-pillar coupling of the above is shown in Fig. 3(a). The figure shows that the mirror reflects the light at a non-90° angle and that the pillar confines the light along its height due to total internal reflection (TIR). At a pillar height of 60 μm, the power was found to be 82.5% or 0.84 dB of the input. The attenuation is primarily due to finite mirror size, mirror location, metallic losses, and diffraction effects. At pillar heights of 105 and 150 μm, the power remained 0.84 dB. This demonstrates that power is confined in the pillar as it propagates along its height. This efficiency compares well with that of 82% or 0.86 dB for a TIR mirror-terminated multimode waveguide beneath a 230-μm diameter lens at a focal length of 780 μm [2]. Fig. 3(b) shows the simulation result when the mirror angle in Fig. 3(a) is changed to 45°. Light remains confined inside the pillar. The coupling efficiency of this configuration is 80.7% or 0.93 dB. If the pillar is removed, and the upper and lower claddings are both oxide for the mirror-waveguide configurations above, the efficiencies are 93% and 91.5% for 45° and 54.74°, respectively. The 45° case has a higher reflectance due to the larger angle of incidence on the mirror and less reflection at the core–cladding interface. In the pillar case, the 54.74° mirror has a higher efficiency because it is rotated

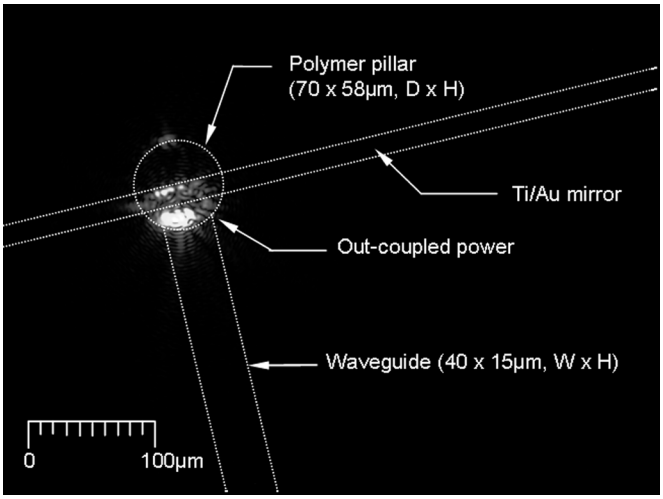

Fig. 4. Microscopic image showing the top view of the experimental waveguide-to-mirror-to-pillar coupling demonstration where light is being coupled out of the pillar due to the gold mirror.

about the center of the waveguide and thus its top edge is closer to the oncoming light and therefore intercepts a larger fraction of that light before it leaks into the pillar. These simulations show that polymer pillars confine the light that is coupled into them, and that there is no inherent coupling penalty incurred by using a non-45° mirror.

IV. Fabrication

A $\langle 100 \rangle$-Si wafer was cleaned and SiO_2 was deposited using plasma enhanced chemical vapor deposition. NR9-8000 photoresist was spun on and rectangles were photolithographically defined. A buffered oxide etch was used to transfer the resist pattern into the SiO_2. The photoresist was removed and the wafer was placed in 25% tetra-methyl-ammonium-hydroxide (TMAH) at 85 °C to transfer the pattern into the Si by etching along its (111)-plane to a depth of 19 μm. The oxide was removed and a 300/2000 Å layer of Ti–Au was selectively sputtered over the etched Si pattern. Titanium promotes adhesion between Au and Si. Next, 2 μm of oxide was deposited onto the wafer to serve as the waveguide substrate cladding. A 15-μm-tall Avatrel film was spun on and channel waveguides were photolithographically defined to terminate at the mirror. A 58-μm-tall Avatrel film was spun on and circular cross sections were photolithographically defined above each mirror-waveguide region. The patterned polymer was hard-baked and spray-developed to yield pillars. The sample was cured at 160 °C for 90 min. Fig. 2 shows a scanning electron microscope (SEM) images of an array of fabricated pillars on mirror-terminated waveguides.

V. Optical Testing

Waveguide-to-mirror-to-pillar coupling was optically tested by coupling light from a single-mode fiber into a 0.5-cm-long waveguide on the Si substrate. Light coupled out of the pillar was observed with a camera located above the pillar. Fig. 4 shows the light propagating in the waveguide being coupled out of the pillar. This figure verifies experimentally that mirrors can be used to couple light into polymer pillars. It also shows that once 54.74° mirrors are integrated with waveguides and pillars, the combination produces a 90° redirecting of the light. Further, it demonstrates that chip-level pillars are compatible with current substrate fabrication technologies. A measured coupling efficiency of between 40% and 50% (3–4 dB) is estimated due to a waveguide loss of between 0.47–10 dB/cm [3], a mirror loss of 0.32 dB, and a scattered light loss inherent in the measurement. In [2], the measured efficiency is 1.3 dB. In our work, the waveguide material is the dominant source of loss (fabrication dependent). A lower-loss material is presently being investigated. The salient message of this letter is that the waveguide-mirror-pillar coupler configuration works.

VI. Conclusion

Optical interconnects represent a potential solution for the I/O bandwidth requirements in future GSI systems. To encourage their use, out-of-plane coupling between the package-substrate and chip must be in a form compatible with electrical packaging and assembly requirements. To this end, spatially confining batch-fabricated polymer pillar optical I/Os were integrated with metallized Si mirror-terminated waveguides and waveguide-to-mirror-to-pillar coupling was simulated and experimentally demonstrated. The simulated coupling efficiency for this unoptimized configuration was 0.84 dB for the 54.74° mirror, which was similar to the 0.93 dB for the 45° mirror. Experimental measurements and optimizations are ongoing. Spatial confinement in the region between a substrate and chip helps maximize device density, compensate for intentional and unintentional deviations from 45° mirrors, and ease substrate technology restrictions.

References

[1] International Technology Roadmap for Semiconductors 2004 update [Online]. Available: http://public.itrs.net/

[2] Y. Ishii and Y. Arai, "Large-tolerant 'OptoBump' interface for interchip optical interconnections," *Electron. Commun. Jpn.*, vol. 86, pt. 2, pp. 1–8, 2003.

[3] A. V. Mulé, R. A. Villalaz, T. K. Gaylord, and J. D. Meindl, "Quasi-free-space optical coupling between diffraction grating couplers fabricated on independent substrates," *Appl. Opt.*, vol. 43, pp. 5468–5475, Oct. 2004.

[4] H. S. Cho, K.-M. Chu, S. Kang, S. H. Hwang, B. S. Rho, W. H. Kim, J.-S. Kim, J.-J. Kim, and H.-H. Park, "Compact packaging of optical and electronic components for on-board optical interconnects," *IEEE Trans. Adv. Packag.*, vol. 28, no. 1, pp. 114–120, Feb. 2005.

[5] A. McCarthy, H. Suyal, and A. C. Walker, "45 degrees out-of-plane turning mirrors for optoelectronic chip carriers based on multimode polymer waveguides," *Eur. Conf. Opt. Commun.*, pp. 808–809, Sep. 2004.

[6] M. S. Bakir, T. K. Gaylord, K. P. Martin, and J. D. Meindl, "Sea of polymer pillars: Compliant wafer-level electrical-optical chip I/O interconnections," *IEEE Photon. Technol. Lett.*, vol. 15, no. 11, pp. 1567–1569, Nov. 2003.

[7] M. S. Bakir, T. K. Gaylord, O. O. Ogunsola, E. N. Glytsis, and J. D. Meindl, "Optical transmission of polymer pillars for chip I/O optical interconnections," *IEEE Photon. Technol. Lett.*, vol. 16, no. 1, pp. 117–119, Jan. 2004.

[8] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, "Nanoimprint lithography," *J. Vac. Sci. Technol. B*, vol. 14, pp. 4129–4133, Nov./Dec. 1996.

[9] C. S. Patel *et al.*, "Silicon carrier with deep through-via, fine pitch wiring, and through cavity for parallel optical transceiver," *Proc. Electron. Comp. Technol. Conf.*, pp. 1318–1324, 2005.

[10] S. H. Song, E. H. Lee, C. D. Carey, D. R. Selviah, and J. E. Midwinter, "Planar optical implementation of crossover interconnects," *Opt. Lett.*, vol. 17, pp. 1253–1255, Sep. 1992.

[11] K. Sakaino and S. Adachi, "Study of Si(100) surfaces etched in TMAH solution," *Sens. Actuators A*, vol. A88, pp. 71–78, Jan. 20, 2001.